Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits

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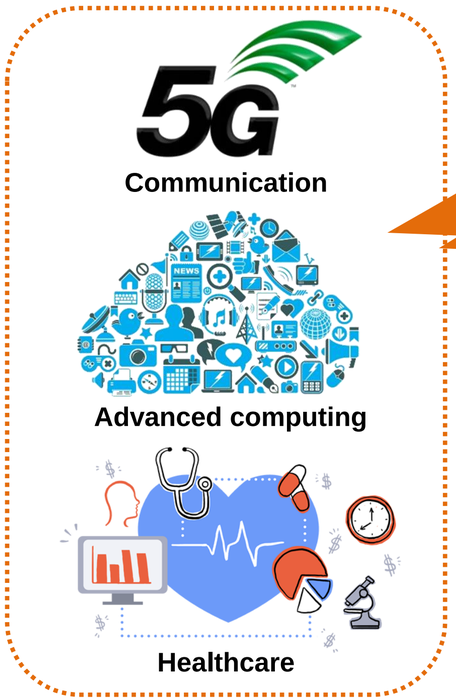
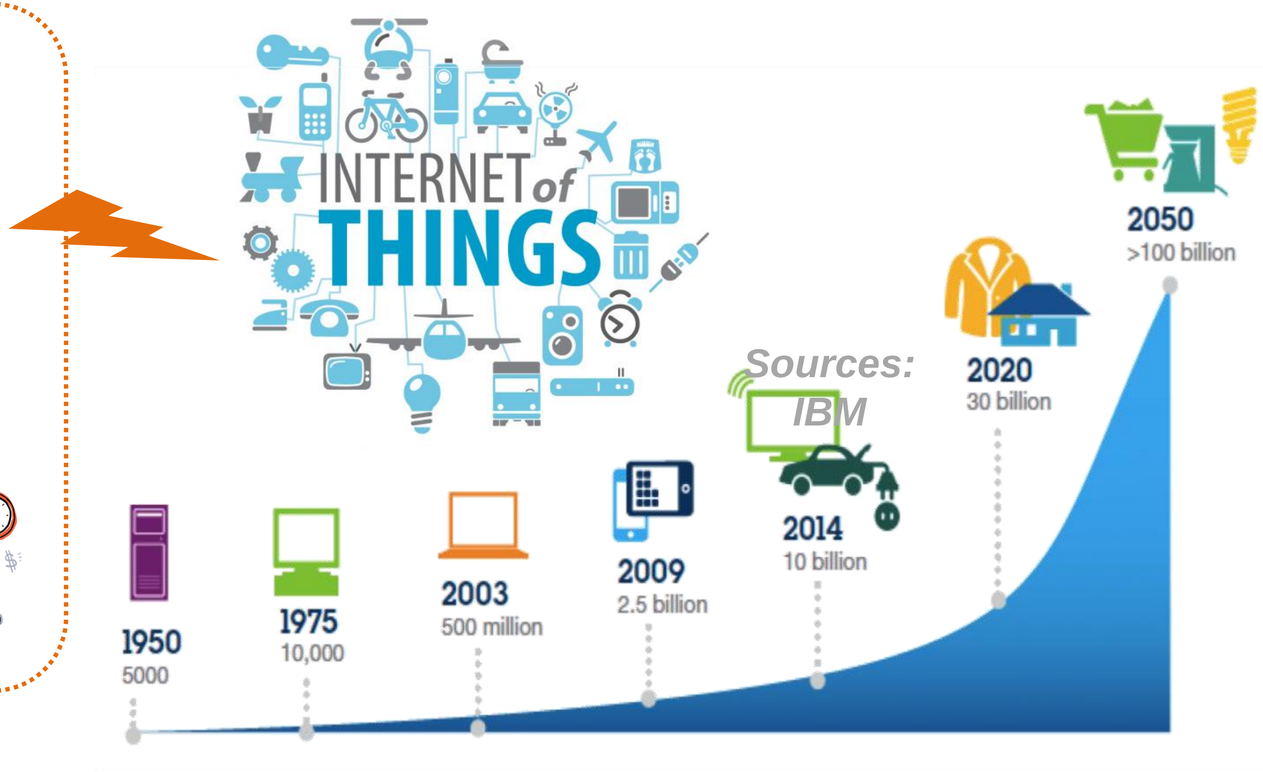
Speaker – Hao Chen

- I am a Ph.D. student in electrical and computer engineering at The University of Texas at Austin.
- I received the B.S. degree in electrical engineering from National Taiwan University (NTU) in 2019.
- Research interests: VLSI physical design and analog/mixed-signal circuit layout synthesis.

High Demand of Analog/Mixed-Signal IC

- Internet of Things (IoT), autonomous and electric vehicles, communication and 5G networks…
- Every sensor-related application needs analog circuits!!



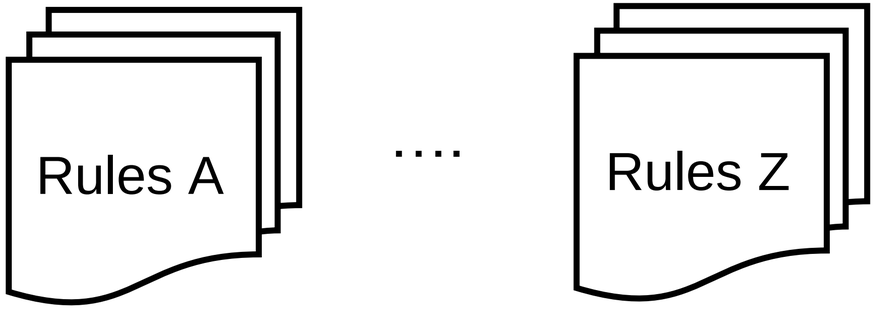


Challenges of Analog Layout Routing

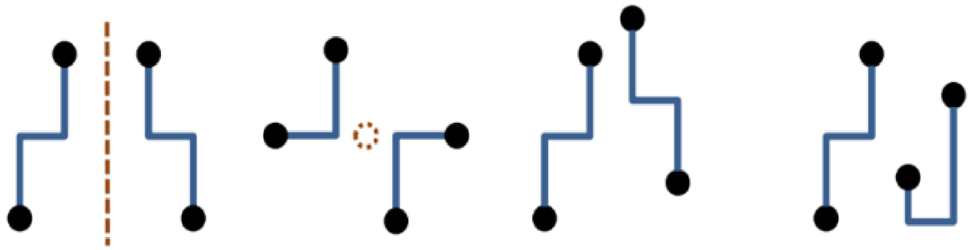
Human experience

Company A

Company Z

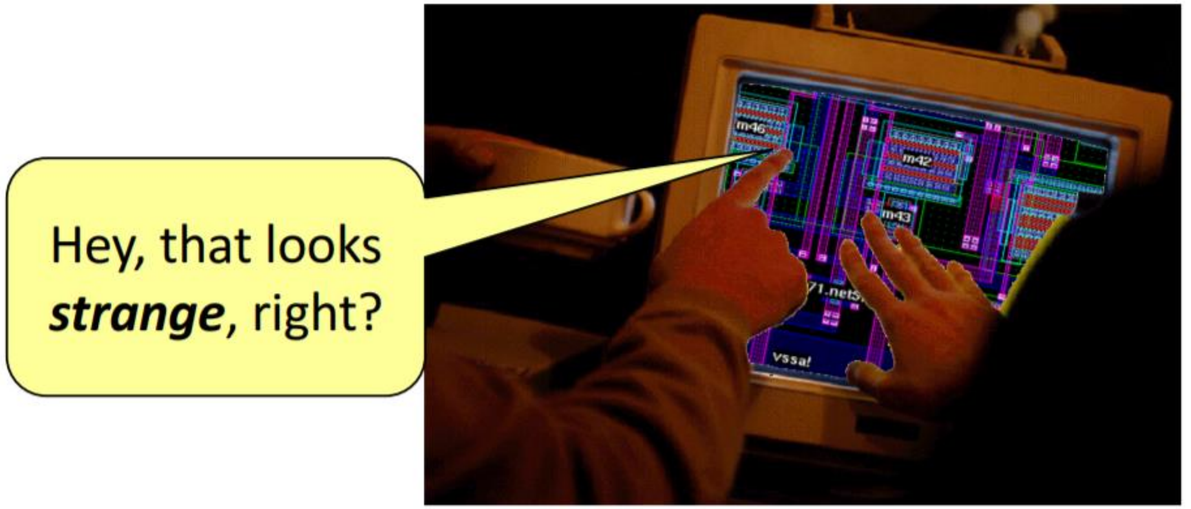


Heuristic constraints



Courtesy of [Ou+, TCAD'14]

Aesthetic engineering

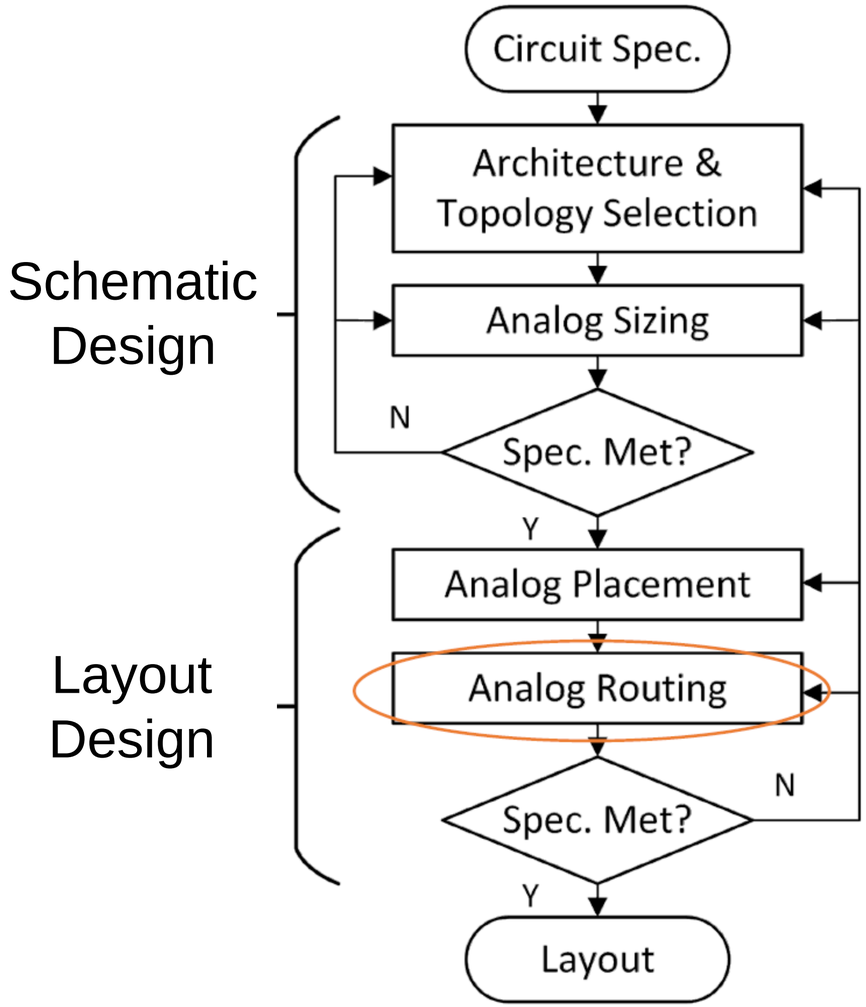


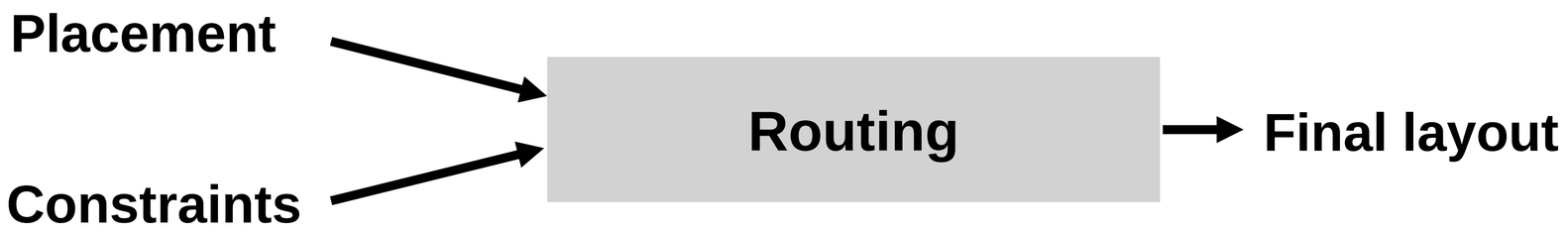
Courtesy of [Rutenbar, TCACE'16]

No comprehensive and exact descriptiveness!!

Typical Automatic Analog Circuit Design Flow

Optimization-based approach

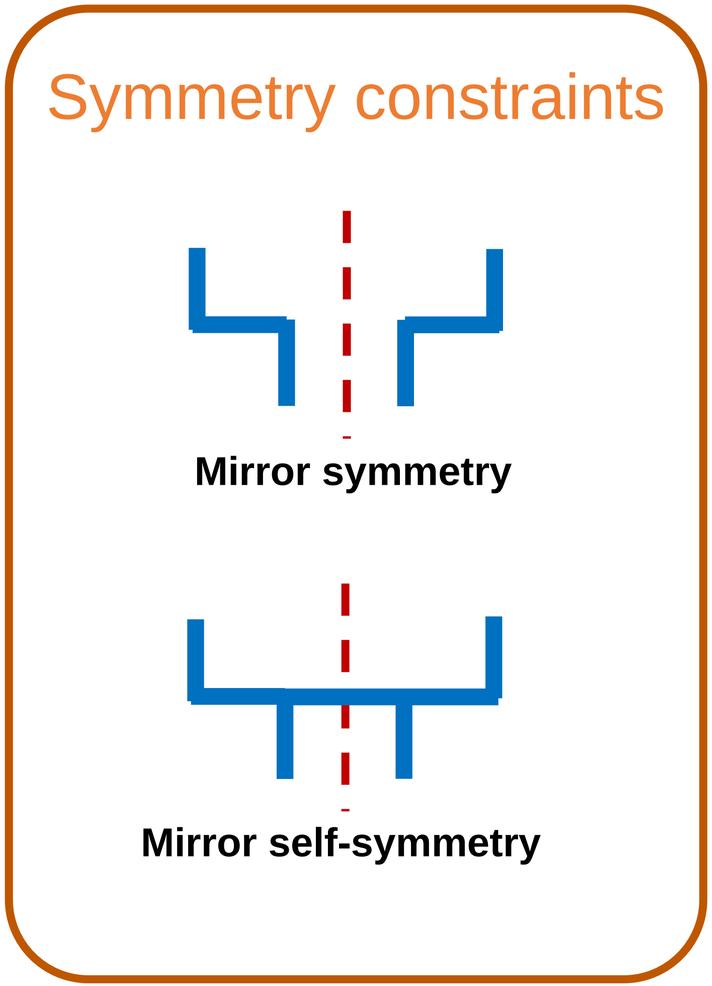


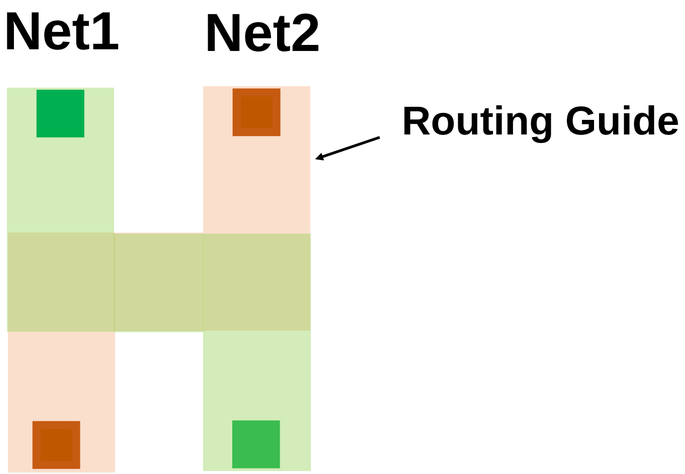


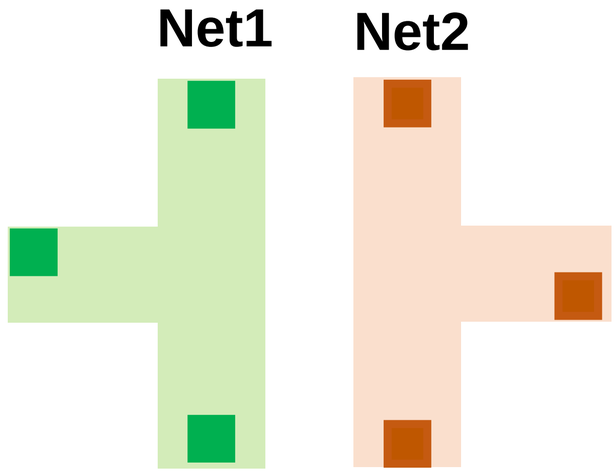
- DRC/LVS clean
- Optimized performance

Analog Routing Constraints

- Symmetry constraints are widely accepted







Cannot be totally symmetric!!

[Xiao+,ICCAD'10][Ou+, TCAD'14][Zhu+, ICCAD'19]…

Analog Routing Constraints

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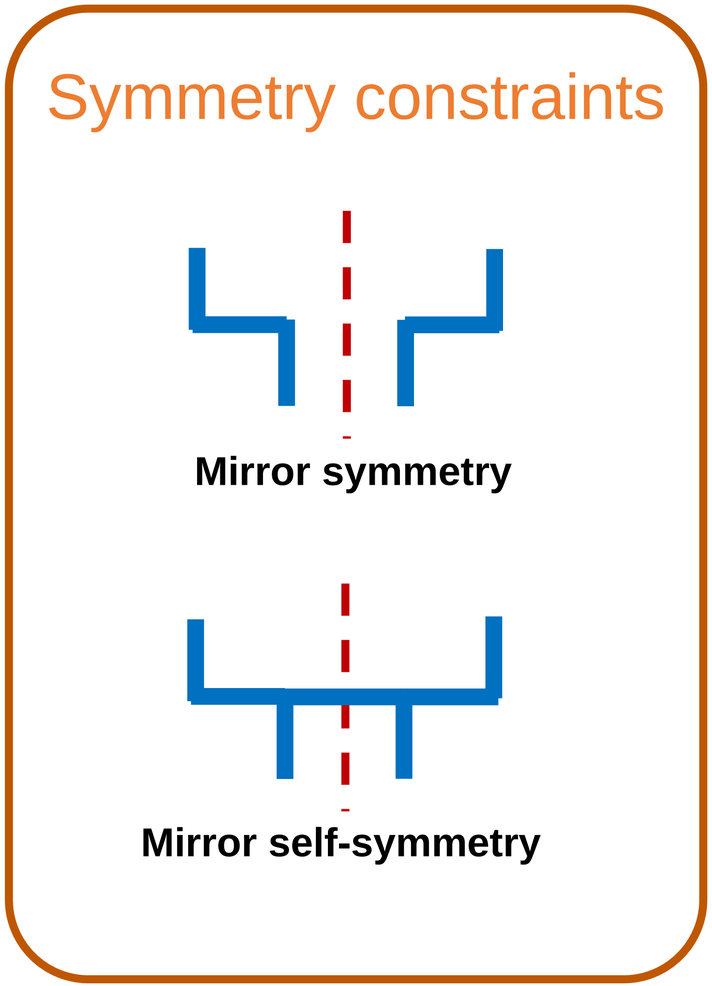
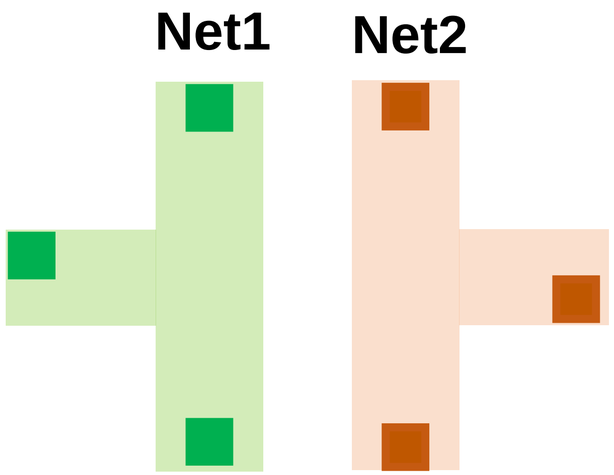
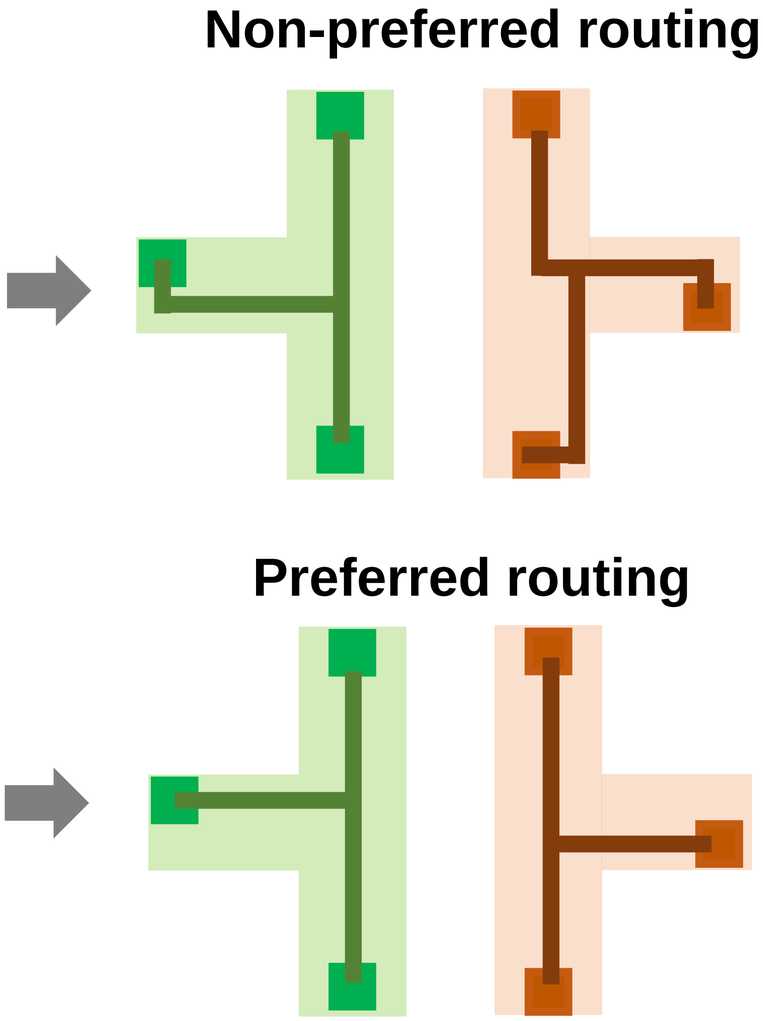


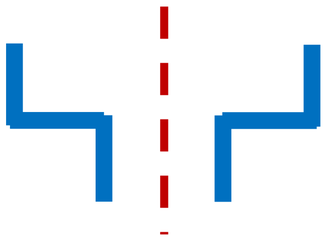




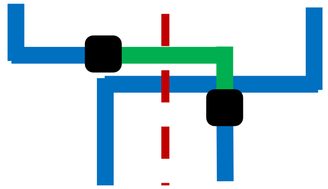
Analog Routing Constraints

Symmetry constraints

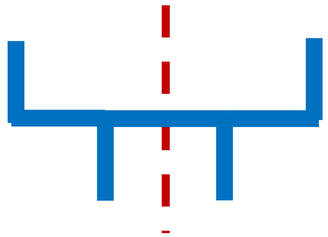
New proposed



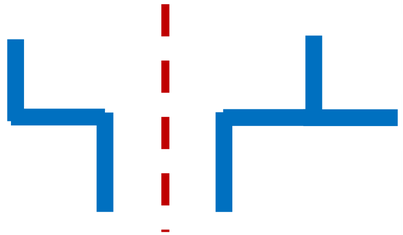
Mirror symmetry



Cross symmetry

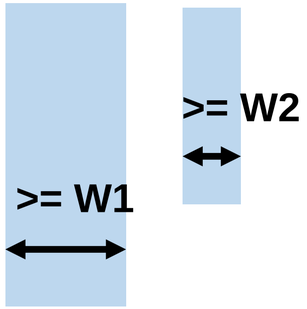


Mirror self-symmetry

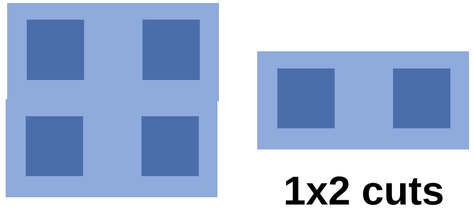


Partial symmetry

Electrical constraints



Metal width lower bound for long wires



2x2 cuts

1x2 cuts

Minimum number of cuts

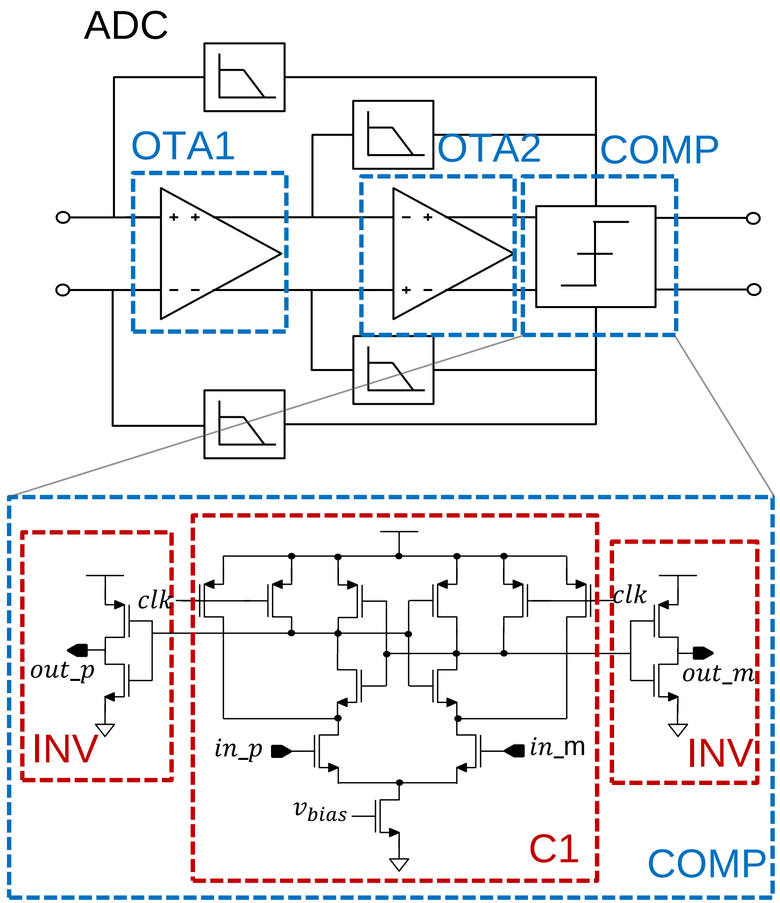
Current matching, balancing

Avoid IR drop issues

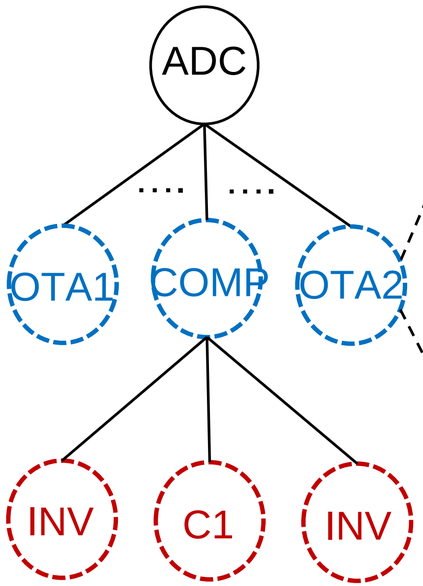
Our AMS Routing Framework

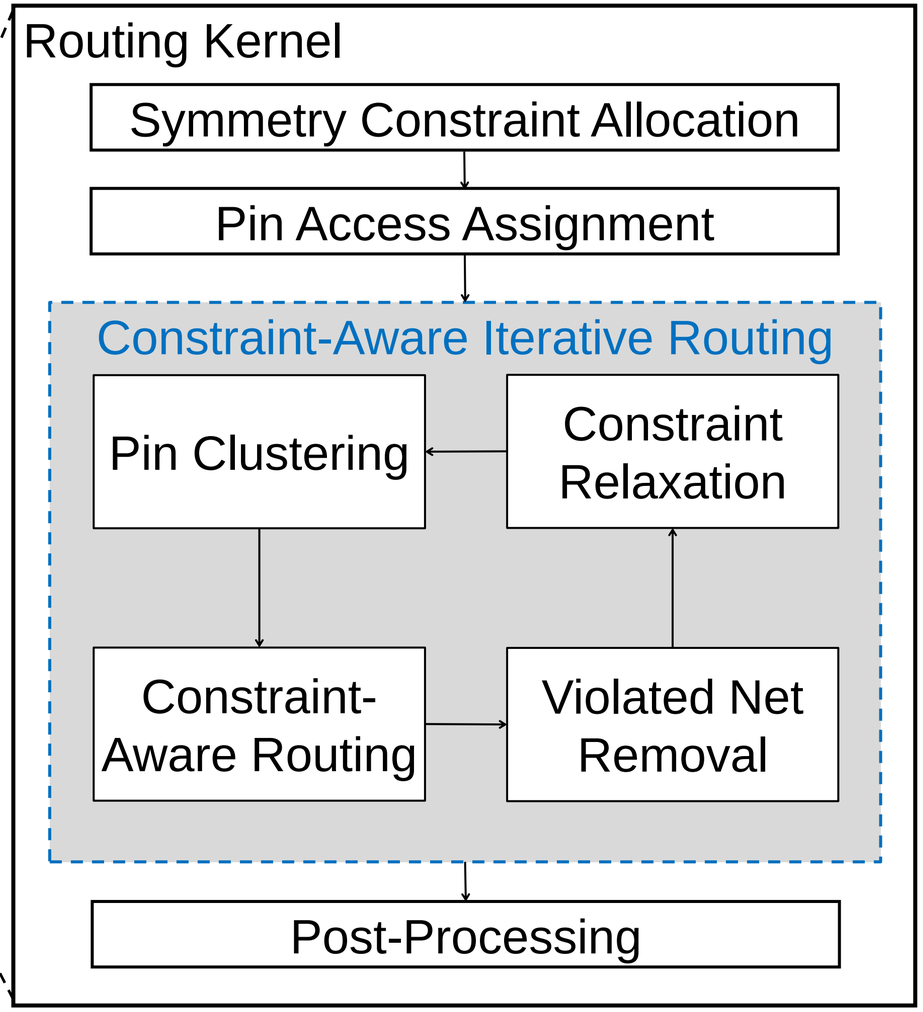
- Repeat the routing process for each node in the hierarchy tree

Circuit schematic



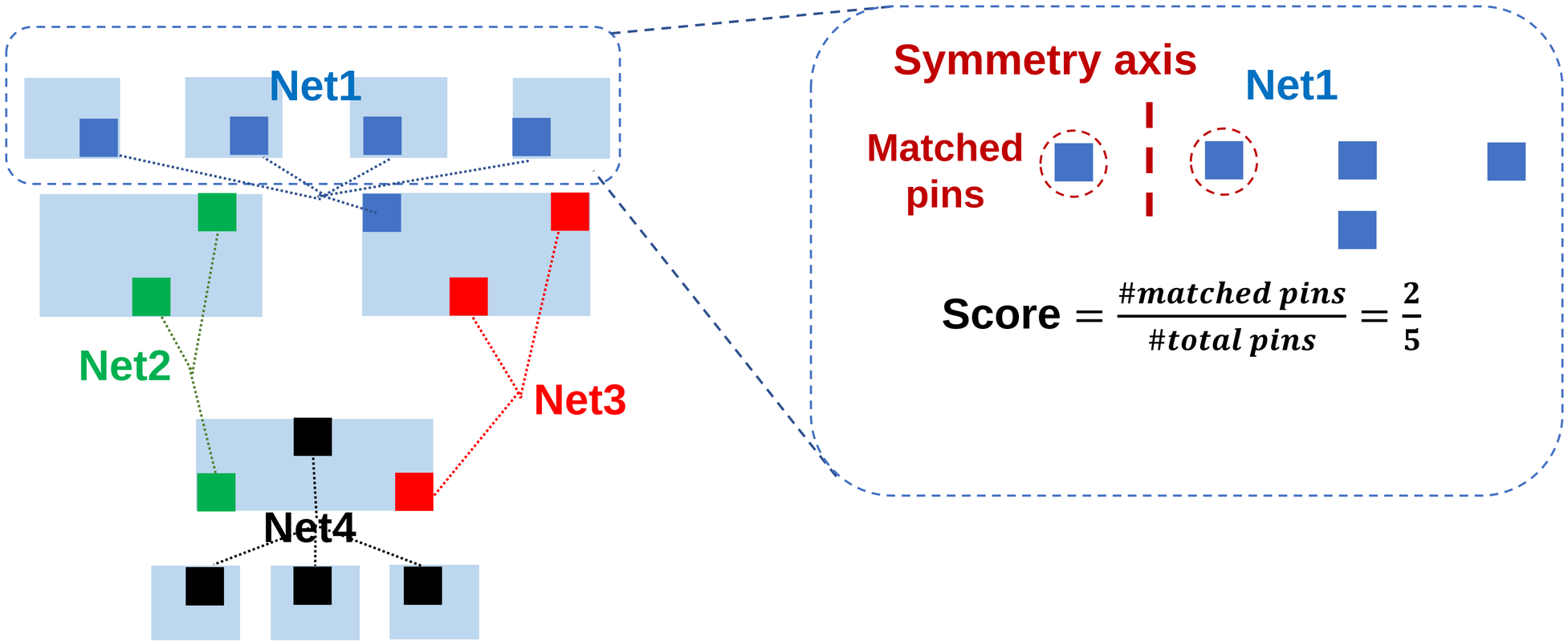
Hierarchy tree





Symmetry Constraint Allocation

- Assign symmetry constraints to nets according to pins locations
- Maximize the overall potential routing symmetry (Weighted graph matching)



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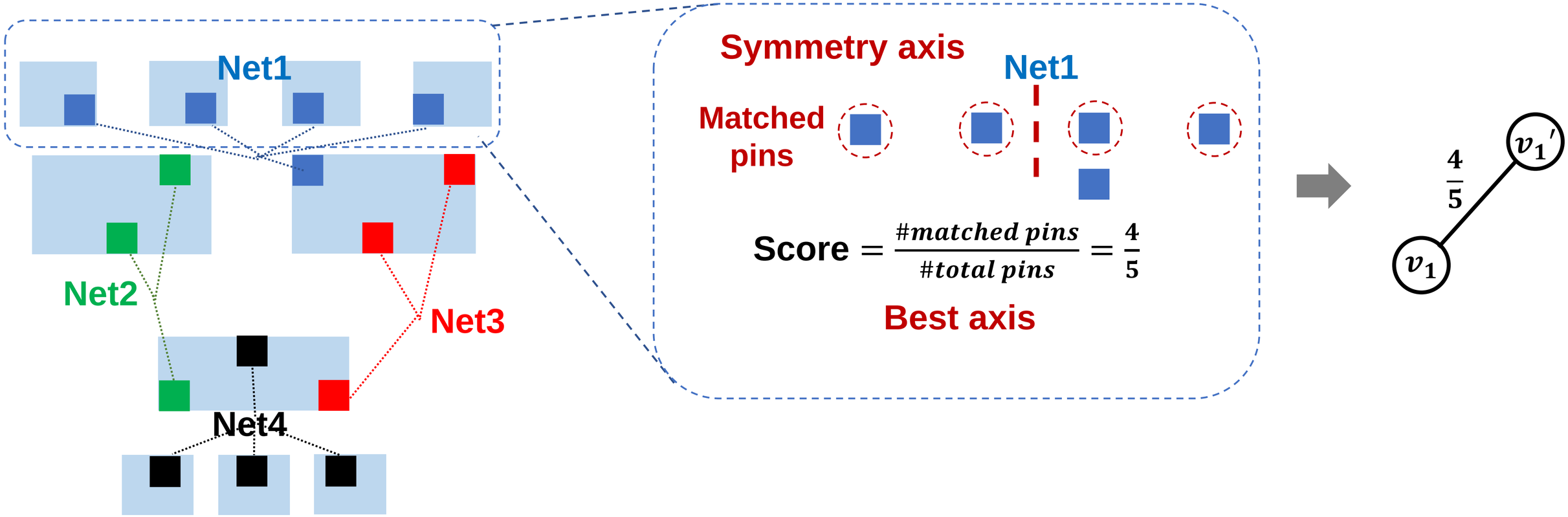

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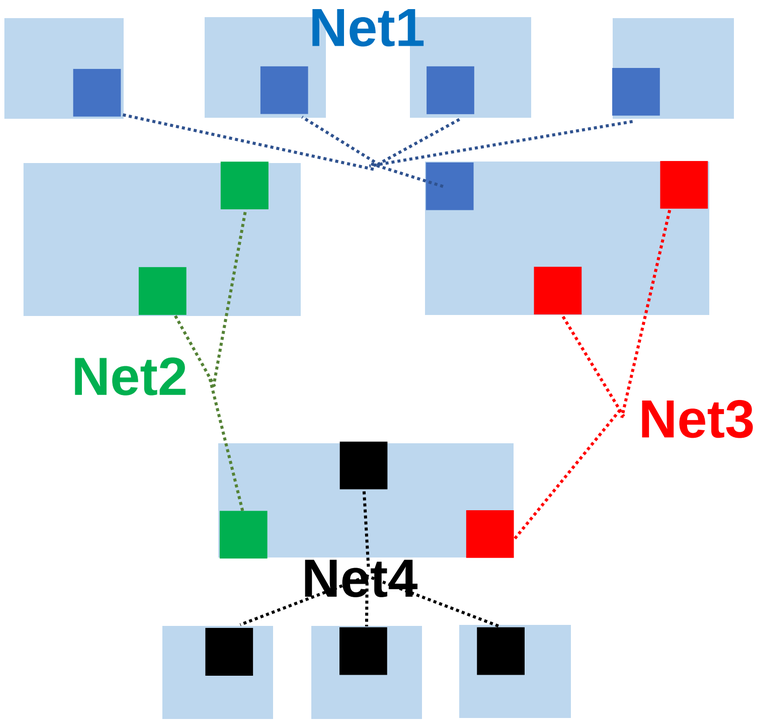

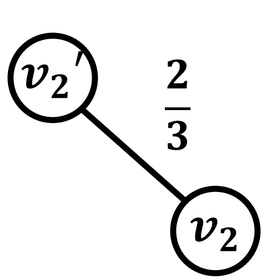

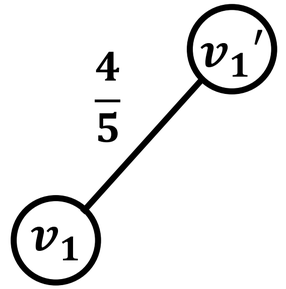

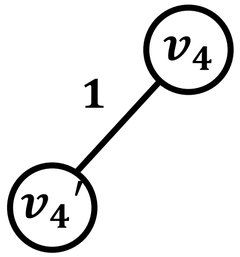

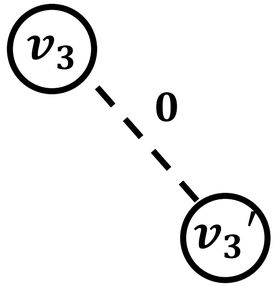

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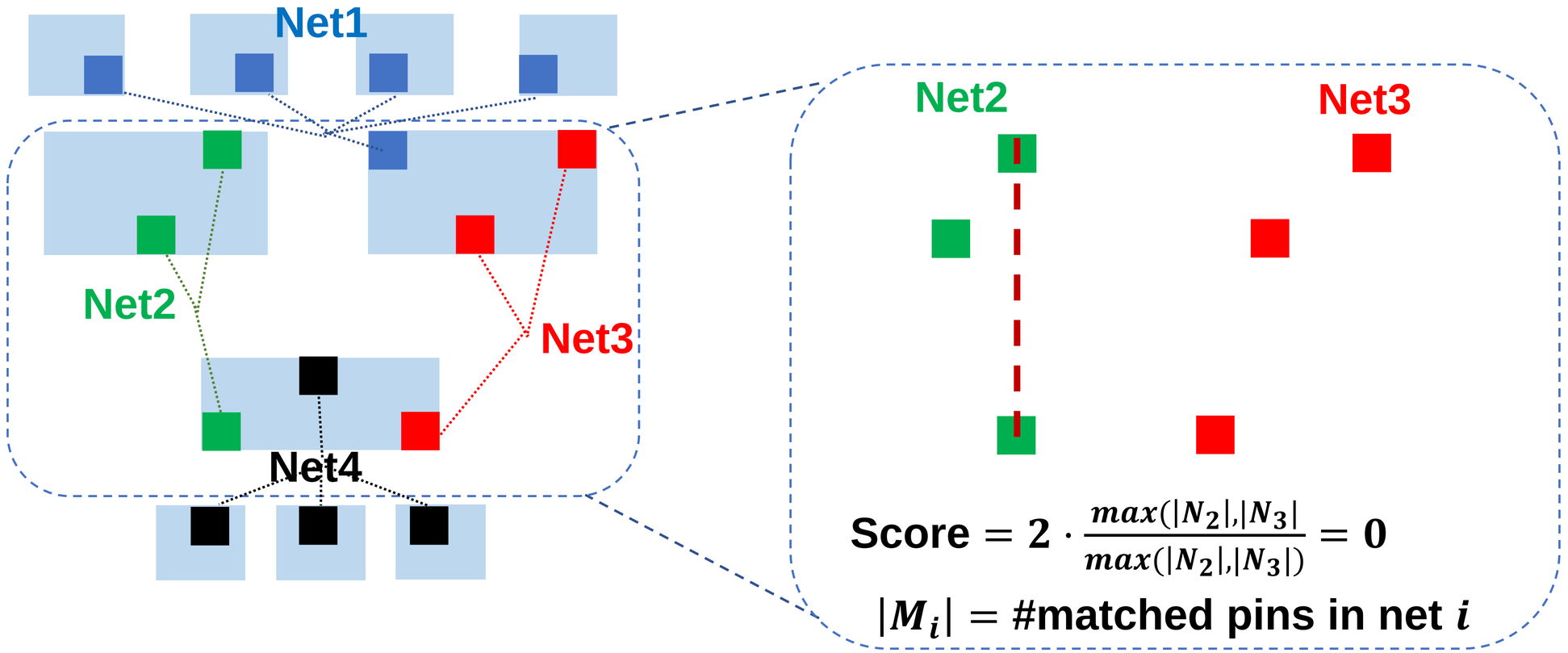

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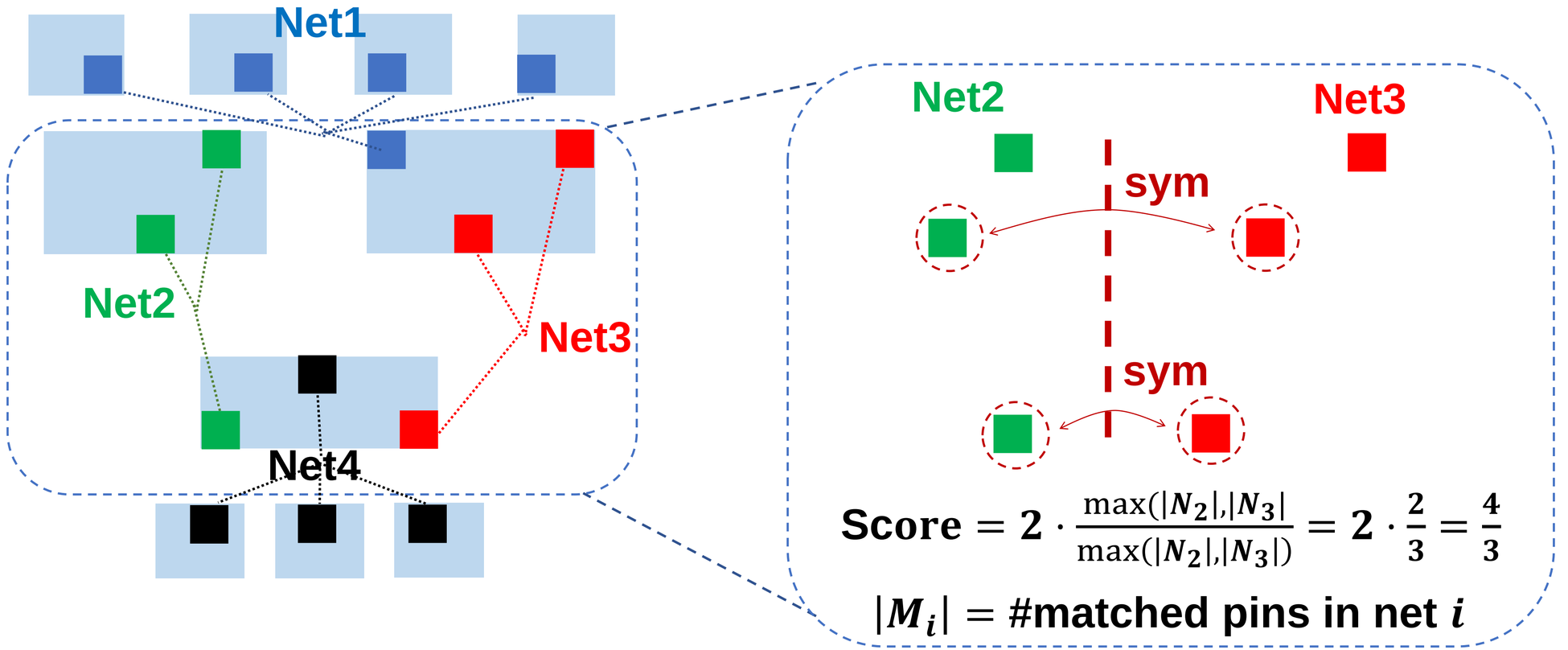

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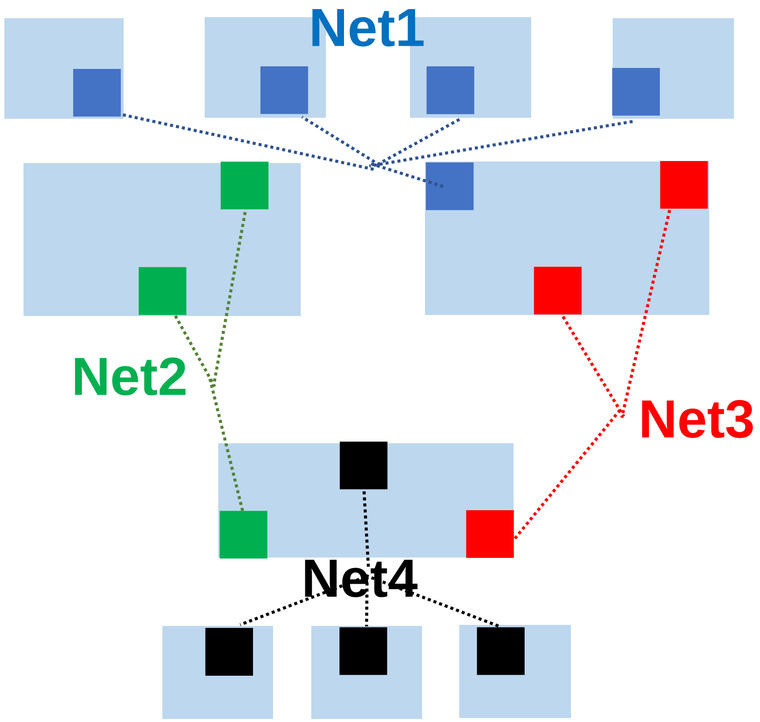

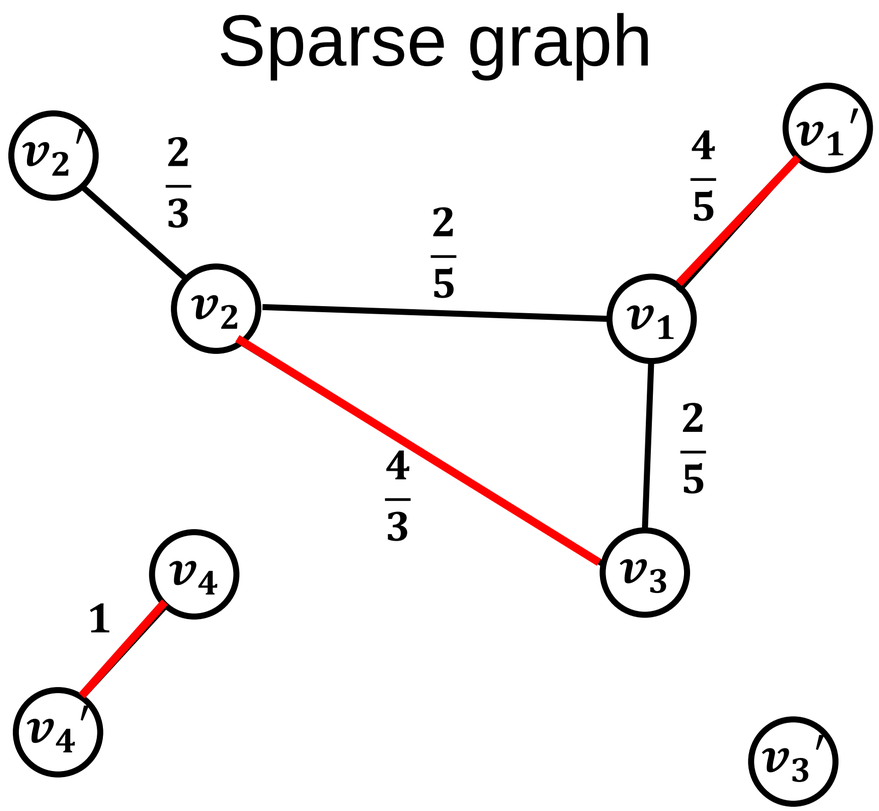

Edmond's blossom algorithm

Symmetry Constraint Allocation

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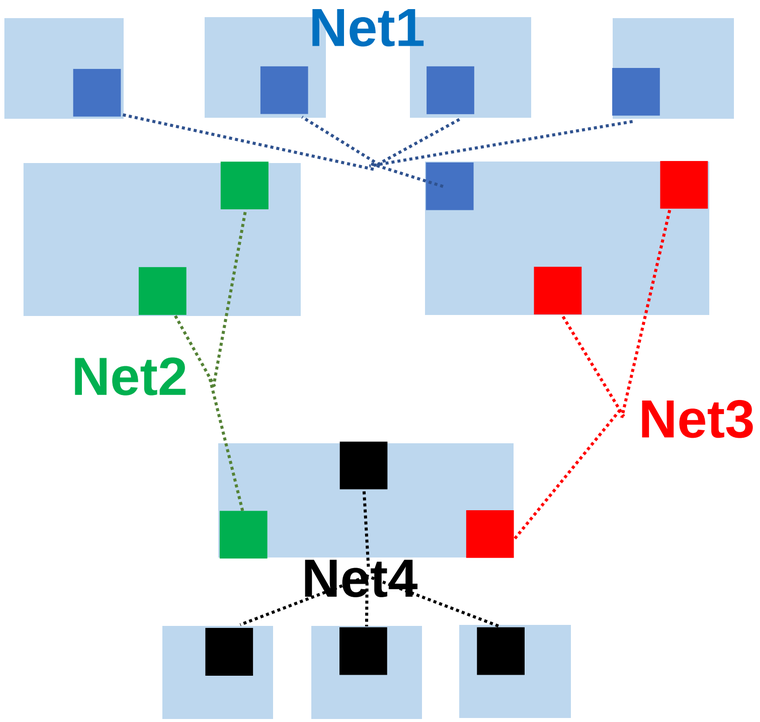
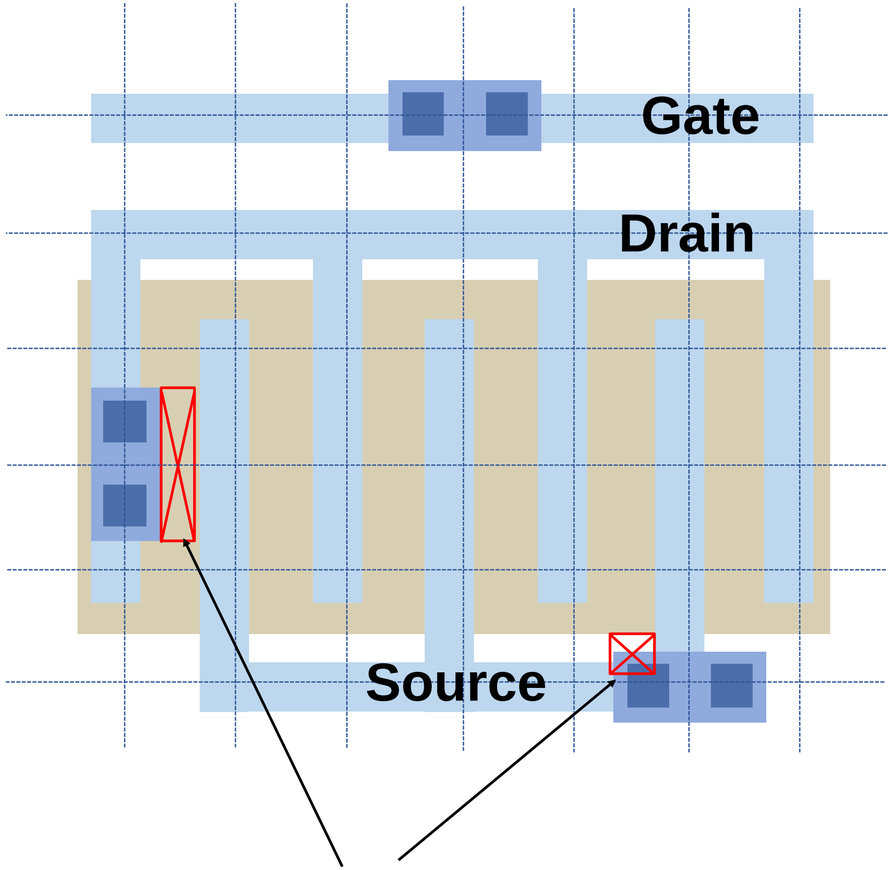


Assigned Constraints

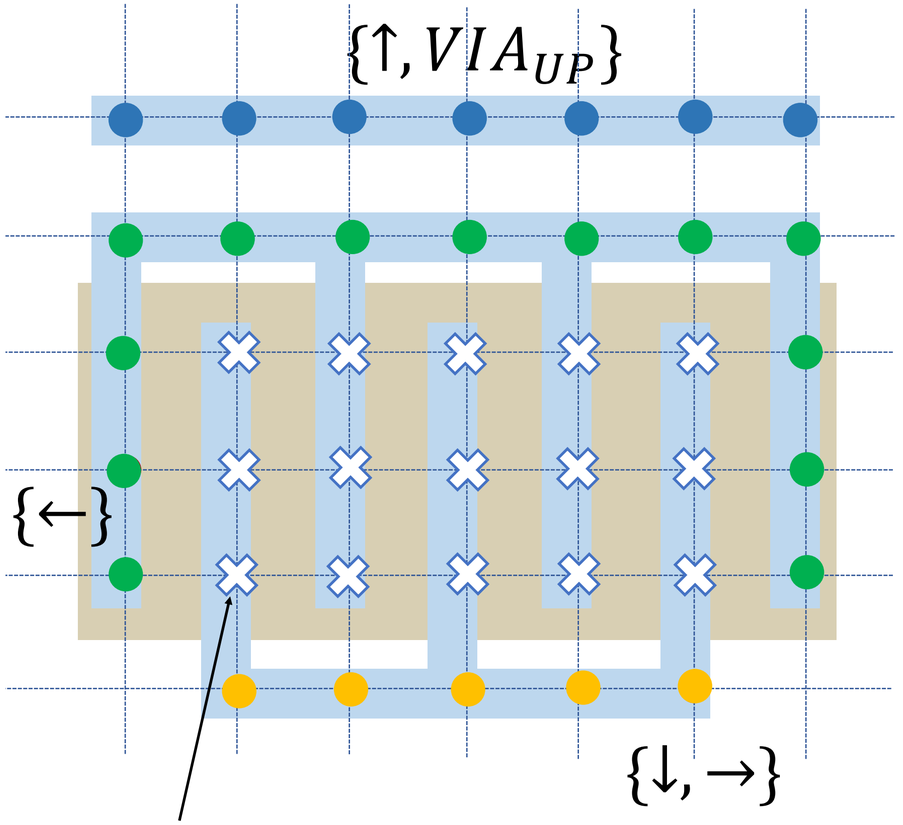
- Net1: self-symmetry
- Net2, Net3: symmetry
- Net4: self-symmetry

Pin Access Assignment

NMOS

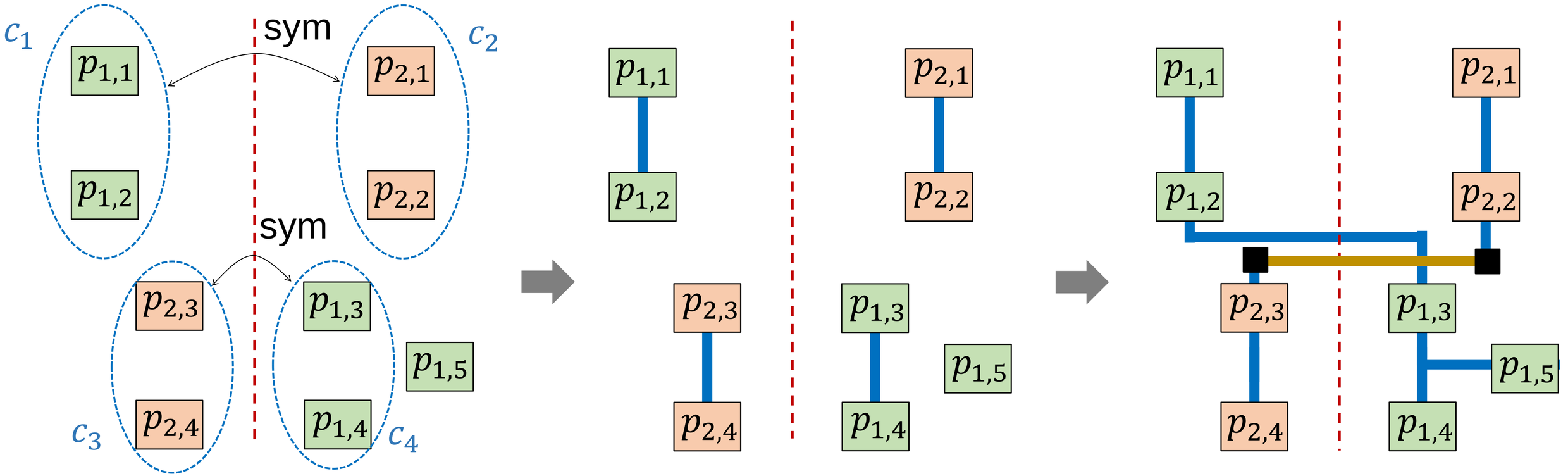


Design rule violations



Invalid points

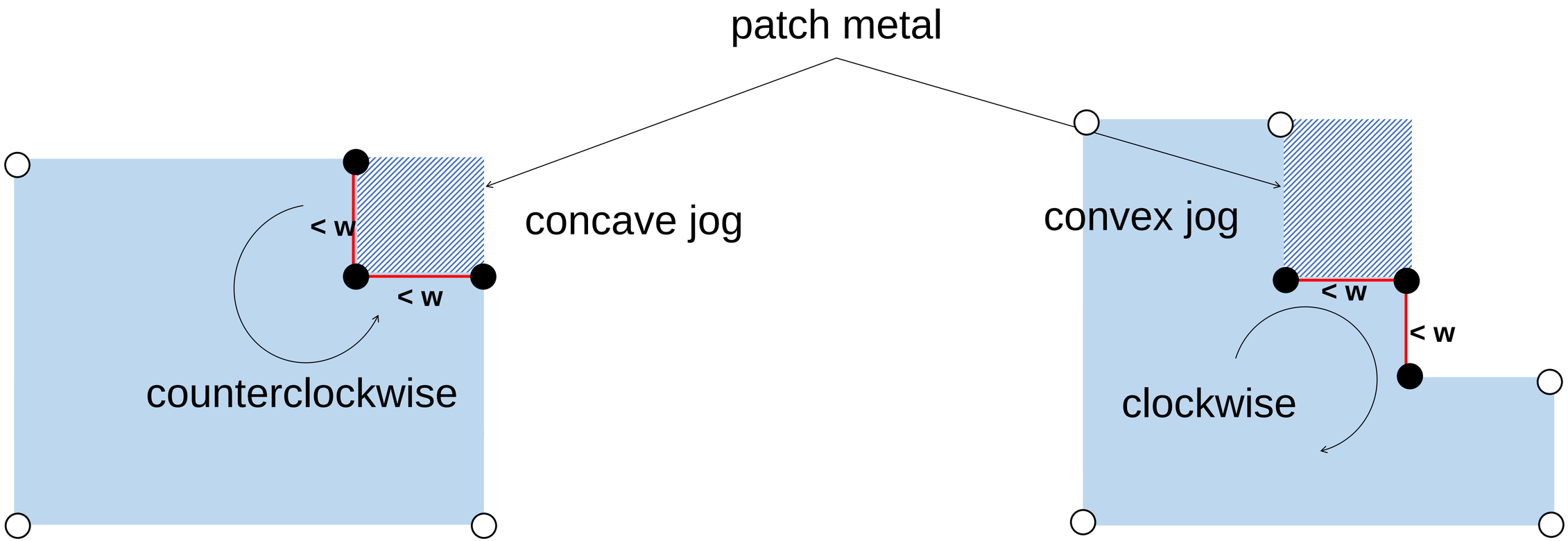
Pin Clustering



$p_{i,j}$: the j^{th} pin of net i

- Find the maximum subset of totally symmetric pins and form clusters
- Connect the pins in each cluster
- Connect the clusters and the remaining pins

Post Processing



Metal patching for design rules

Experimental Results

Setup
- C++ with Boost, Lemon
- CPU: Intel i9-7900X @ 3.3GHz

Benchmark circuits
- COMP: comparator
- OTA1: Miller compensation OTA
- OTA2: 2-stage feedforward compensation OTA
- ADC1: 2nd-order CT ΔΣ modulator
- ADC2: 3rd-order CT ΔΣ modulator

[Zhu+, ICCAD'19]

Benchmark	WL	VIA	Sym Deg.	DRV	Runtime (s)
COMP	145.67	90	0.37	83	1.34
OTA1	520.64	167	0.31	170	36.30
OTA2	546.88	191	0.19	130	15.18
ADC1	2898.84	498	0.37	550	39.65
ADC2	N/A	N/A	N/A	N/A	N/A
Norm.	1.13	3.60	0.40	-	24.75

This work

Benchmark	WL	VIA	Sym Deg.	DRV	Runtime (s)
COMP	138.40	19	0.95	**0**	0.11
OTA1	386.80	38	0.88	**0**	1.71
OTA2	523.40	79	0.70	**0**	0.37
ADC1	2686.60	175	0.62	**0**	2.70
ADC2	3327.60	184	0.69	**0**	18.82
Norm.	1.00	1.00	1.00	**-**	1.00

13% WL reduction
DRC clean
24X speedup

Experimental Results

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ADC1 simulation result

Metrics	Schematic	[Zhu+, ICCAD'19]	This work
Fs (MHz)	320		
BW (MHz)	5		
SNDR (dB)	67.7	63.0	**63.5**
SFDR (dB)	84.8	78.0	**81.7**
Power (uW)	838.1	842.6	858.0

OTA2 simulation result

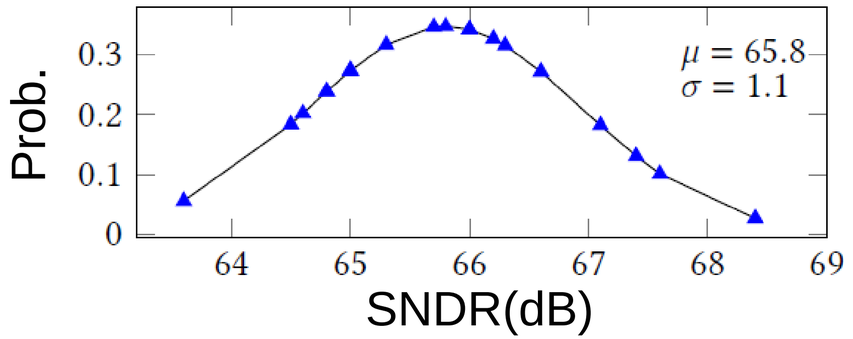
Metrics	Schematic	[Zhu+, ICCAD'19]	This work
DC Gain (dB)	54.0	52.9	**54.1**
BW (MHz)	605.2	444.8	**477.0**
PM (degree)	64.1	75.3	**76.1**
Offset (uV)	-	893.3	**145.7**
Noise (uVrms)	12070.1	9711.5	9822.1
Power (uW)	428.7	424.3	439.7

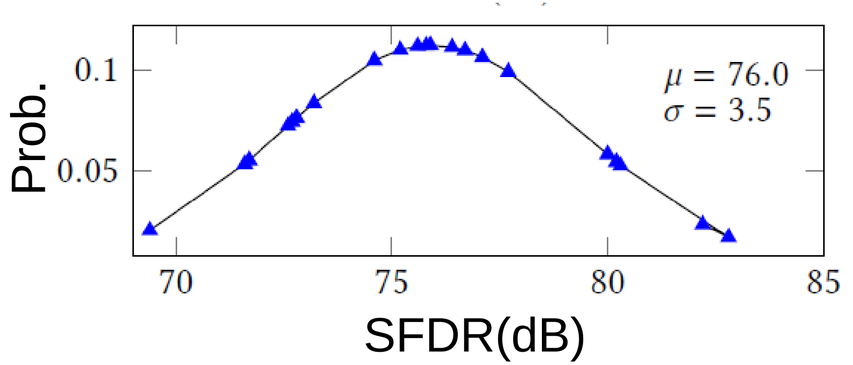
Experimental Results (ADC2)

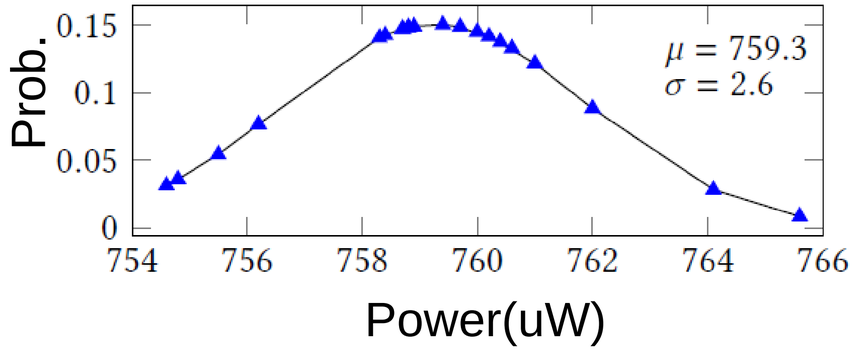
PVT simulation

Corner	SNDR(dB)	SFDR(dB)	Power(uW)
TT-N	66.1	79.8	759.0
TT-C	67.4	80.8	747.8
TT-H	64.3	78.3	774.7
FF-C	71.9	83.5	812.2
FF-H	65.4	82.7	854.4
SS-C	62.4	77.8	679.8
SS-H	62.1	76.8	711.9

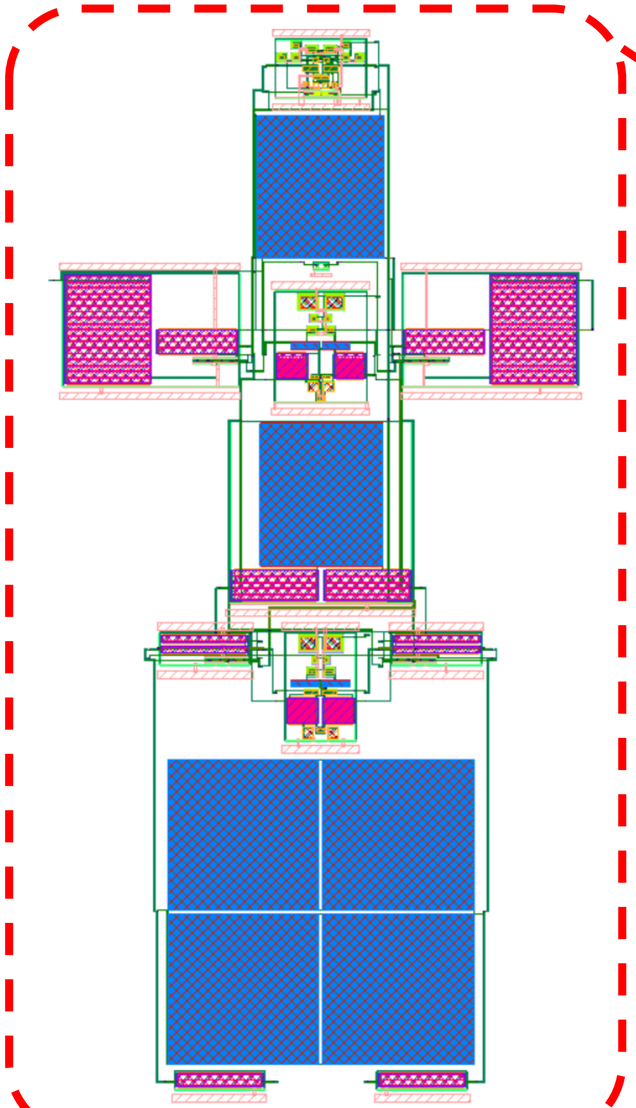
Monte-Carlo simulation



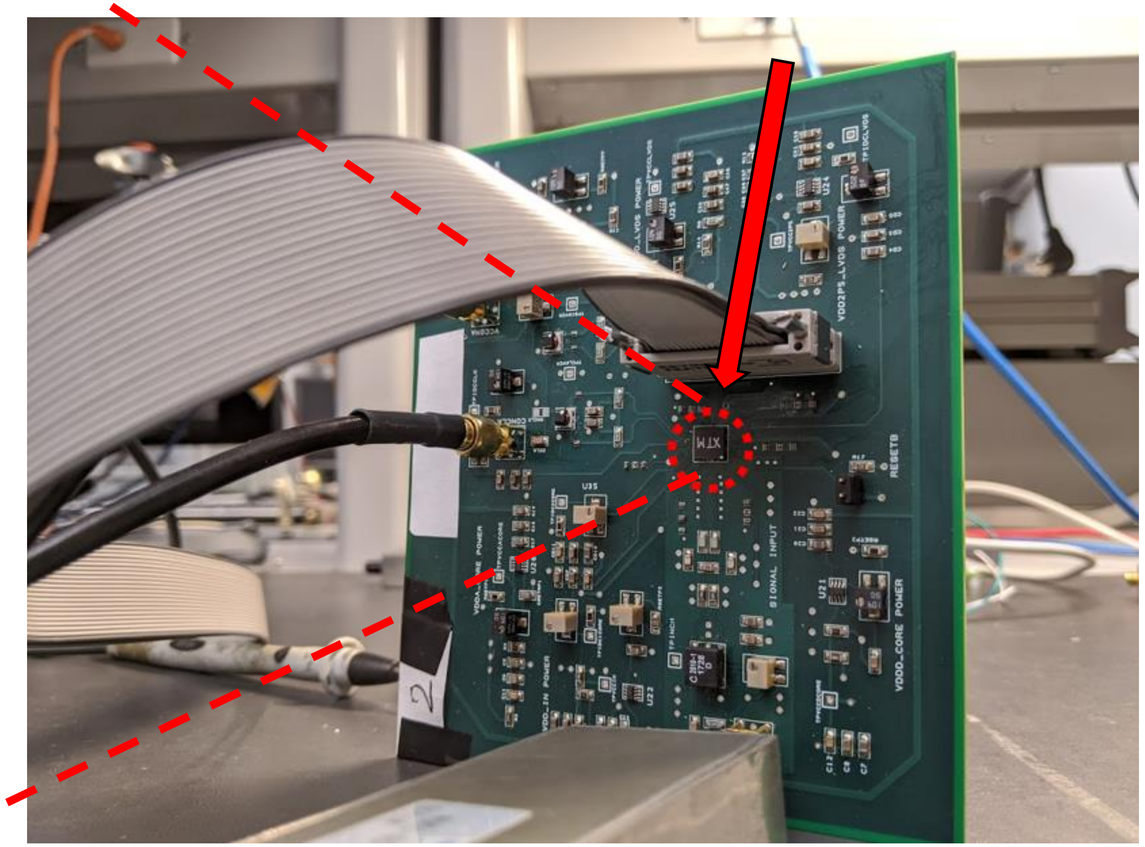




Experimental Results (ADC2)



ADC2



Taped-out and in measurements!!

Conclusions

AMS Router

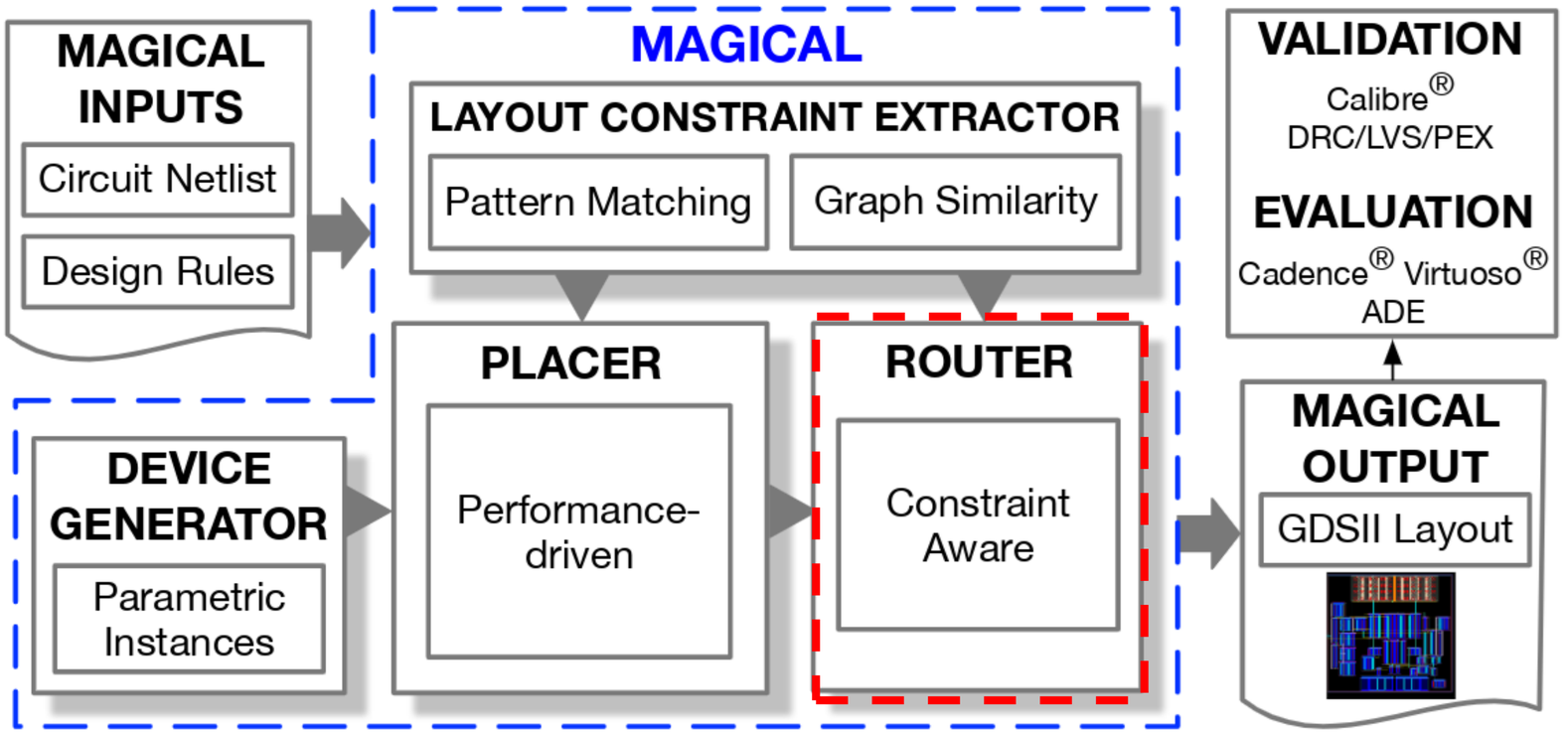
- Symmetry constraint allocation
- Pin Access Assignment
- Hierarchical routing scheme for large/complicated systems with pin clustering
- Sign-off quality layout (DRC/LVS clean, performance guaranteed)

Future directions

- Advanced technology nodes (FinFET)
- Extended circuit classes

Machine Generated Analog IC Layout (MAGICAL)

- This work is part of the MAGICAL project
- End-to-end analog layout automation system
- Open source at Github: https://github.com/magical-eda/MAGICAL



Thank you!