KEREN ZHU

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RESEARCH INTERESTS

Electronic Design Automation (EDA)

- Design automation for analog and mixed-signal (AMS) circuits
- Artificial intelligence (AI) for EDA
- Placement and routing (PNR) algorithms
- CAD for emerging computing

EDUCATION

The University of Texas at Austin, TX, USA *Aug. 2016 – June 2022*
Ph.D., Department of Electrical and Computer Engineering
Advisor: David Z. Pan
Dissertation title: *Fully-Automated Layout Synthesis for Analog and Mixed-Signal Integrated Circuits*

University of Wisconsin-Madison, WI, USA *Sep. 2012 – May. 2016*
B.S.E.E. with Highest Distinction, Department of Electrical and Computer Engineering
GPA 3.97/4.0

PROFESSIONAL EXPERIENCE

The Chinese University of Hong Kong, HK SAR, China *March 2023 –*
Research Assistant Professor
Department of Computer Science

The University of Texas at Austin, TX, USA *June 2022 – Feb. 2023*
Postdoctoral Fellow
Department of Electrical and Computer Engineering

Nvidia Inc., TX, USA *May 2021 – May 2022*
Internship
ASIC and VLSI Research Group: Design Automation

Cerebras System, CA, USA *May 2020 – Oct. 2020*
Internship
Software Stack: Place and Route

Apple, TX, USA *May 2018 – Aug. 2018*
Internship
SOC: Physical Design

SELECTED RESEARCH PROJECTS

Machine Generated AMS IC Layout
MAGICAL software for automated AMS layout generation [C2, C10, J1, J3]

- Open-source https://github.com/magical-eda/MAGICAL
- World's first practical AMS layout automation proven in silicon on a real-world circuit

Analytical placement algorithm [C7, C15, C17, J5]
Efficient routing algorithm [C1, C8, C21]
Automated constraint extractions from the netlist with statitical methods [C3, C13, C19]
Netlist-to-GDSII fully automated flow [C5, C10, C14]
Machine-learning guided physical design and analog layout performance modeling [C1, C4, C15, C17, C19]

AI-Enhanced EDA Algorithms
ML-guided PNR algorithms [C1, C4, C15]
Hyper-parameter optimization in EDA [C5, C22]
Reinforcement learning in EDA [C9, C16, C21]
Circuit modeling and representation learning [C13, C17, C20]

AWARDS AND HONORS

PhD Forum *2022*
IEEE/ACM Design Automation Conference (DAC)

Best Student Paper Award Nomination *2021*
IEEE Custom Integrated Circuits Conference (CICC)

Best Paper Award Nomination *2020*
IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)

Harry Philip Whitworth Endowed Graduate Fellowship *2021*
The University of Texas at Austin

Hilldale Undergraduate/Faculty Research Fellowship *2015*
University of Wisconsin-Madison

Hugo Jr. and Pennie Longemann Scholarship *2014*
University of Wisconsin-Madison

Vincent Rideout Scholarship *2013*
University of Wisconsin-Madison

PROFESSIONAL SERVICE

TPC Member

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023.
- Design Automation conference (DAC), 2023.
- International VLSI Design & Embedded Systems conference (VLSID), 2023.

Session (Co-)Chair

- Session "Efficient AI for the Edge: From Head to Toe!", DAC, 2023.
- Session "Novel EDA for Analog Designs", ISEDA, 2023.
- Session "Novel Placement and Routing Algorithms", ISEDA, 2023.

Program Committee Member

- PhD Forum@DAC, 2023.

Session Organizer

- Tutorial *Reinforcing Circuit and Layout Synthesis* at DAC 2023.
- TILOS Early Career Development in Industry Panel, 2023

Session Chair/Moderator

- Session *Efficient AI for the Edge: From Head to Toe!* at DAC 2023.
- Workshop *SIGDA Early Career Workshop* at DAC 2023.
- TILOS Early Career Development in Industry Panel, 2023, YouTube

Working Group Member

- NSF AI Institute TILOS Ethics and Early Career Development, 2022-2023.

Local Arrangement Co-Chair

- IEEE CASS Seasonal School: AI/ML for IC Design and EDA, 2022.

Reviewer

IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

ACM Transactions on Design Automation of Electronic Systems (TODAES)

IEEE Transaction on Artificial Intelligence (TAI)

IEEE Transactions on Circuits and Systems I (TCAS-I)

ACM/IEEE Design Automation Conference (DAC)

IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

Neural Information Processing Systems (NeurIPS)

IEEE International Symposium on Low Power Electronics and Design (ISLPED)

Integration, the VLSI Journal

TEACHING

Other teaching activities:

Guest Lecture	EE382M: VLSI CAD and Optimization	UT Austin	Spring 2023
Teaching Assistant	EE382M: VLSI CAD and Optimization	UT Austin	Fall 2018
Teaching Assistant	ECE230: Circuit Analysis	UW-Madison	Fall 2015

MENTORING

Supervised senior undergraduates for capstone project UT, 2021
Title: "MAGICAL: ML for Automated Analog IC Layout"
Mentees: Mina Gawargious, Jason Juliette, Justin Ko and Lang Zhou

Served as Mentor for First-Year Graduate Students UT, 2021
UT ECE Graduate Partner Program
Mentees: Gillian Yost, Lekhaj Patha, Yancheng Du and Weiran Huang

SKILLS

Programming Languages
C/C++, Python

EDA Tools
Cadence Innovus, Synopsys Design Compiler, Synopsys Prime Time

PUBLICATIONS

Books/Book Chapters

[B2b] Steven M. Burns, Hao Chen, Tonmoy Dhar, Ramesh Harjani, Jiang Hu, Nibedita Karmokar, Kishor Kunal, Yaguang Li, Yishuang Lin, Mingjie Liu, Meghna Madhusudan, Parijat Mukherjee, David Z. Pan, Jitesh Poojary, S. Ramprasath, Sachin S. Sapatnekar, Arvind K. Sharma, Wenbin Xu, Soner Yaldiz, and **Keren Zhu**, "Machine Learning for Analog Layout," in *Machine Learning Applications in Electronic Design Automation*, edited by Haoxing Ren and Jiang Hu, Springer, 2022. (Authors in alphabetic order)

[B2a] Ahmet F. Budak*, Shuhan Zhang*, Mingjie Liu, Wei Shi, **Keren Zhu**, and David Z. Pan, "Machine Learning for Analog Circuit Sizing," in *Machine Learning Applications in Electronic Design Automation*, edited by Haoxing Ren and Jiang Hu, Springer, 2022.

[B1] Mohamed B. Alawieh, Ahmet F. Budak, Hao Chen, Mingjie Liu, David Z. Pan, Wei Shi, Xiyuan Tang, Shuhan Zhang and **Keren Zhu**, "CAD for Analog/Mixed-Signal Integrated Circuits," in *Advances in Semiconductor Technologies: Selected Topics Beyond Conventional CMOS*, edited by An Chen, Wiley-IEEE Press, 2022. (Authors in alphabetic order)

Journal Papers

[J6] Xiangxing Yang, **Keren Zhu**, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun,, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," in *IEEE Journal of Solid State Circuits (JSSC)*, 2023

[J5] **Keren Zhu**, Hao Chen, Mingjie Liu and David Z. Pan, "Hierarchical Analog and Mixed-Signal Circuit Placement Considering System Signal Flow," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.

[J4] Mingjie Liu*, Xiyuan Tang*, **Keren Zhu**, Hao Chen, Nan Sun, and David Z. Pan, "1MS/s and 80MS/s SAR ADCs in 40nm CMOS with End-to-End Compilation," in *IEEE Solid-State Circuits Letters*, 2023. (* indicates equal contributions in alphabetic order)

[J3] **Keren Zhu**, Hao Chen, Mingjie Liu and David Z. Pan, "Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System," in *IEEE Transactions on Circuits and Systems II*, 2022.

[J2] Hao Chen*, Mingjie Liu*, Xiyuan Tang* **Keren Zhu***, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," in *Journal of Semiconductors*, 2020. (* indicates in alphabetic order, Invited) **Featured on Cover**

[J1] Hao Chen*, Mingjie Liu*, Biying Xu* **Keren Zhu***, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," in *IEEE Design & Test*, 2020. (* indicates equal contributions in alphabetic order, Invited)

Conference Papers

[C25] Zehua Pei, Fangzhou Liu, Zhuolun He, Guojin Chen, Haisheng Zheng, **Keren Zhu** and Bei Yu, "AlphaSyn: Logic Synthesis Optimization with Efficient Monte Carlo Tree Search," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, October 29 - November 2, 2023.

[C24] Ahmet F. Budak, **Keren Zhu** and David Z. Pan, "Practical Layout-Aware Analog/Mixed-Signal Design Automation with Bayesian Neural Networks," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, October 29 - November 2, 2023.

[C23] Hyunsu Chae, Bhyrav Mutnury, **Keren Zhu**, Doug Wallace, Doug Winterburg, Daniel DeAraujo, Jay Reddy, Adam Klivans and David Z. Pan, "ISOP: Machine Learning-Assisted Inverse Stack-Up Optimization for Advanced Package Design," in *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Antwerp, Belgium, April 17 - 19, 2023.

[C22] Ahmet F. Budak, **Keren Zhu**, Hao Chen, Souradip Poddar, Linran Zhao, Yaoyao Jia and David Z. Pan, "Joint Optimization of Sizing and Layout for AMS Designs: Challenges and Opportunities," in *ACM International Symposium on Physical Design (ISPD)* , March 26 - 29, 2023. (Invited)

[C21] Hao Chen, Kai-Chieh Hsu, Walker J. Turner, Po-Hsuan Wei, **Keren Zhu**, David Z. Pan and Haoxing Ren, "Reinforcement Learning Guided Detailed Routing for FinFET Custom Circuits," in *ACM International Symposium on Physical Design (ISPD)* , March 26 - 29, 2023.

[C20] **Keren Zhu**, Hao Chen, Walker Tuner, George Kokai, Po-Hsuan Wei, David Z. Pan and Haoxing Ren, "TAG: Learning Circuit Spatial Embedding From Layouts," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, July 10-14, 2022. **Best Paper Candidate Nominated from Track**

[C19] Hanqing Zhu, **Keren Zhu**, Jiaqi Gu, Harrison Jin, Ray T. Chen, Jean Anne Incorvia, and David Z. Pan, "Fuse and Mix: ACAM-Enabled Analog Activation for Energy-Efficient Neural Acceleration," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Francisco, CA, July 10-14, 2022.

[C18] Hao Chen, Walker J. Turner, Sanquan Song, **Keren Zhu**, George F. Kokai, Brian Zimmer, C. Thomas Gray, Brucek Khailany, David Z. Pan, and Haoxing Ren, "AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies," in *ACM International Symposium on Physical Design (ISPD)* , Virtual Conference, March 27-30, 2022. (Invited)

[C17] **Keren Zhu**, Hao Chen, Mingjie Liu and David Z. Pan, "Automating Analog Constraint Extraction: From Heuristics to Learning," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022. (Invited)

[C16] Ahmet F. Budak*, Zixuan Jiang*, **Keren Zhu**, Azalia Mirhoseini, Anna Goldie, and David Z. Pan, "Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022. (* indicates equal contributions in alphabetic order)

[C15] **Keren Zhu**, Hao Chen, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, "Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Virtual Conference, January 17-20, 2022.

[C14] Mingjie Liu, Xiyuan Tang, **Keren Zhu**, Hao Chen, Nan Sun, and David Z. Pan, "OpenSAR: An Open Source Automated End-to-end SARADC Compiler," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Conference, November 1-5, 2021.

[C13] Hao Chen, **Keren Zhu**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," in *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, December 5-9, 2021.

[C12] Zixuan Jiang, Jiaqi Gu, Mingjie Liu, **Keren Zhu**, and David Z. Pan, "Optimizer Fusion: Efficient Training with Better Locality and Parallelism," in *International Conference on Learning Representations (ICLR) Workshop, Hardware Aware Efficient Training (HAET)*, May 07, 2021.

[C11] Xiangxing Yang, **Keren Zhu**, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. **Best Student Paper Award Nomination**

[C10] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, **Keren Zhu***, Abhishek Mukherjee, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1 GS/s $\Delta\Sigma$ ADC," in *IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, April 25-30, 2021. (* indicates equal contributions in alphabetic order)

[C9] **Keren Zhu**, Mingjie Liu, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," in *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, November 16-20, 2020.

[C8] Hao Chen, **Keren Zhu**, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, November 02-05, 2020.

[C7] **Keren Zhu**, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, November 02-05, 2020. **Best Paper Candidate Nominated from Track**

[C6] Zixuan Jiang, **Keren Zhu**, Mingjie Liu, Jiqi Gu, and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," in *European Conference on Computer Vision (ECCV)*, Glasgow, United Kingdom, August 23-27, 2020.

[C5] Mingjie Liu, **Keren Zhu**, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis," in *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, July 19-23, 2020.

[C4] Mingjie Liu*, **Keren Zhu***, Jiqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning," in *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020. (* indicates equal contributions in alphabetic order)

[C3] Mingjie Liu, Wuxi Li, **Keren Zhu**, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S^{3}DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity," in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)*, Beijing, China, January 13-16, 2020. **Best Paper Award Nomination**

[C2] Biying Xu, **Keren Zhu**, Mingjie Liu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, November 4-7, 2019. (Invited)

[C1] **Keren Zhu**, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Routing Paradign Using Generative Neural Network Guidance for Analog Circuits," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, November 4-7, 2019. **Best Paper Candidate Nominated from Track**